The University of Texas at Tyler
Department of Electrical Engineering

Course: EENG 4331.002,041, CMPE 4331.001, 040 – VLSI Design

Syllabus

Catalog Description:

MOS transistor theory; CMOS manufacturing technology; Design and fabrication of digital integrated circuits; EDA tools for design of VLSI circuits; Physical Design Flow; Low Power IC Design; Design rules for VLSI Design; CMOS Logic Design; datapath circuits and subsystem design issues; Testing and verification of Integrated circuits. Three hours of lecture each week.

Prerequisites: EENG 3302 Digital Systems, EENG 3306 Electronic Circuit Analysis I

Credits: 3 (3 hours lecture, 0 hours laboratory per week)

Text(s): N. H. E. Weste and D. Harris. *CMOS VLSI Design.* 4th Edition. Pearson-Addison-Wesley, 2011. ISBN 978-0321-547743

Additional Material: Class Notes; Journal Articles; Online resources

Course Coordinator: Prabha Sundaravadivel, AssociateProfessor

Topics Covered: (paragraph of topics separated by semicolons)

VLSI CAD Tools; Fabrication of Integrated Circuits; Modeling Submicron Transistors; Static and Dynamic Logic Gate Design; Datapath design; Subsystem design; Delay, Power Characterization; Clock Distribution; Physical Design; Interconnect Modelling; Testing and Verification Issues.

Evaluation Methods: (only items in dark print apply):

1. Examinations / Quizzes
2. Homework
3. Report
4. Computer Programming
5. Project
6. Presentation
7. Course Participation
8. Peer Review

Course Learning Outcomes[1]: By the end of this course students will be able to:

1. Describe the processing steps for creating a CMOS Integrated Circuit. [1,2]
2. Analyze different operating regions for MOSFET through current equations. [1,2]
3. Model digital circuits using Register-to-Transfer Logic (RTL) programming. [4,5]
4. Design a static CMOS Logic gate. [1]
5. Analyze different nanoscale devices. [1]
6. Optimize the device sizing for a complex logic circuit using the concept of logical effort. [1,2]
7. Determine the delay in CMOS circuits. [1]
8. Characterize a CMOS logic gate utilizing SPICE simulation data. [4,5]
9. Implement transistor-level schematic of compound CMOS logic gates. [2]
10. Assess the design challenges of implementing dynamic logic circuits in submicron technologies. [1]
11. Analyze different memory architectures in the transistor-level. [1,2]
12. Identify the issues with testing complex logic circuits. [1,2]
13. Understand the issues with designing devices and circuits using nanotechnology. [1]
14. Describe the steps involved in physical design flow. [1,7]
15. Explore the current research trend in VLSI Design. [6]

[1] *Numbers in brackets refer to method(s) used to evaluate the course learning outcome.*

Relationship to Student Outcomes (only items in dark print apply)[2]: This course supports the following Electrical Engineering Student Outcomes, which state that our students will possess:

1. An ability to identify, formulate, and solve complex engineering problems by applying principles of engineering, science, and mathematics [1,2,9,10].
2. An ability to apply engineering design to produce solutions that meet specified needs with consideration of public health, safety, and welfare, as well as global, cultural, social, environmental, and economic factors [4,5,6,11,12].
3. An ability to communicate effectively with a range of audiences [15].
4. An ability to recognize ethical and professional responsibilities in engineering situations and make informed judgments, which must consider the impact of engineering solutions in global, economic, environmental, and societal contexts [14].
5. an ability to function effectively on a team whose members together provide leadership, create a collaborative and inclusive environment, establish goals, plan tasks, and meet objectives
6. An ability to develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgment to draw conclusions [3,8].
7. An ability to acquire and apply new knowledge as needed, using appropriate learning strategies. [13].

[2]*Numbers in brackets refer to course learning outcome(s) that address the Program Outcome.*

Contribution to Meeting Professional Component: (in semester hours)

Mathematics and Basic Sciences:		hours
Engineering Sciences and Design:	3	hours
General Education Component:		hours

Grade Replacement:

If you are repeating this course for a grade replacement, you must file an intent to receive grade forgiveness with the registrar by the 12th day of class. Failure to file an intent to use grade forgiveness will result in both the original and repeated grade being used to calculate your overall grade point average. A student will receive grade forgiveness (grade replacement) for only three (undergraduate student) or two (graduate student) course repeats during his/her career at UT Tyler. (2006-08 Catalog, p. 35)

Prepared By:	Prabha Sundaravadivel	Date:	22 August 2018
Edited By:			

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COURSE OUTLINE

Course Coordinator:

Dr. Prabha Sundaravadivel,
Associate Professor, Department of Electrical and Comp. Engineering
Office: RBN 2015
Email: PSundaravadivel@uttyler.edu
Office Hours: Monday 11:00 – 2 PM
Email and Discussion Boards.

Class Location/Time: Synchronous Zoom classes (**HEC**) and in-person (**Tyler – RBN 2011**).
Monday 5 – 7:50 PM
Zoom link:
https://uttyler.zoom.us/j/92348252912?pwd=8R1KvIbfeZuiS7JFpba95hbYVnJ9Na.1
Passcode: Fall2025

Grading Policy:

Homework	15%	No. of Homework - 3
Participation	5%	Engagement through Discussion Boards and email
Labs/ Mini Projects	20%	No. of. Assignments – 4
Reading Assignments	10%	2 Research Papers
Mid Term Exam	20%	October 6 2025
Final Exam	30%	November 16, 2025
Total	**100%**	

Semester Schedule:

Week	Date	Topics	Homework	Lab/ Mini Project
1	Aug 25	Course Overview, Introduction to VLSI CMOS Logic Gates, CMOS Manufacturing		
2	Sept 1	MOS Transistor Theory, MOSFET I-V and C-V Characteristics	**Hw1**	
3	Sept 8	Introduction to Verilog and EDAs (LT SPICE)	**Hw1 due**	**Lab 1**
4	Sept 15	CMOS Design issues		**Lab 1 due**

5	Sept 22	Power Estimation, Interconnect Modeling	**Hw2**	
6	Sep 29	Low Power Design, Delay Characterization	**HW-2 due**	
7	Oct 6	**Mid-Term Exam**		
8	Oct 13	Combinational Circuit Design, Static and Dynamic Logic Circuit Families		**Lab 2**
9	Oct 20	Sequential Circuit Design		**Lab 2 due**
10	Oct 27	Datapath Subsystem		**Lab 3**
11	Nov 2	Memory Design	**Hw 3**	**Lab 3 due**
12	Nov 9	Design for Testing, Verification	**Hw 3 due**	**Lab 4**
13	Nov 16	**Final Exam**		
14	Nov 23			
15	Nov 30	Physical Design Review		**Lab 4 due**
16	Dec 06	Research Paper Review		

Mode of Delivery:
The semester will begin with synchronous zoom classes for students joining from HEC (.040) and in-person classes for students joining from Tyler (.001). Students are expected to log in through Zoom to attend the lectures and attend in person depending upon their registered sections. At the end of each class, the recorded lectures will be posted in Canvas. If the student has any concerns or would like to share their feedback on the lectures, email the Instructor anytime.

Flexible Online Office Hours:
This course will have extended office hours. Students can meet with the Instructor during the office hours on Mondays (11-2 PM) using the course zoom link. However, if students are not available during the mentioned office hours, they are strongly encouraged to schedule a meeting with the Instructor anytime.

Homework:
There will be a total of 3 assignments. Homeworks will be in the form of problems, theory questions, and a take home quiz to test the understanding of basic concepts. Homework will be assigned by Monday as per the schedule and will be due on Friday of the following week. No late homework will be accepted. Homework problems/ questions may be discussed with other students, but the final submission should be an original and independent solution.

Lab/Mini Project:
Four labs or mini projects will be assigned throughout the semester. The topics to be covered here are: Verilog programming and Circuit design. The following software are to be used for the lab assignments:

1. LTSpice - http://www.analog.com/en/design-center/design-tools-and-calculators/ltspice-simulator.html

Research Reading Assignments:
Two research papers will be assigned by the Mid-Term week. Students are expected to read them and make a 10-minute presentation for each paper. This presentation can be done during the regular class meeting time. The total of 20-minute presentation will have 10% weightage.

Exam:

This course will have MidTerm and Final exam. The MidTerm exam will have 20% weightage and Final exam will have a 30% weightage.

Academic Integrity:
Students should be aware that absolute academic integrity is expected of every student in all undertakings at the University of Texas at Tyler. A plagiarism check will be done all the reports submitted by students. Copied or unoriginal solutions will result in a "0" in that course component. Use of Generative AI is not allowed for completing the reports. Evidence of a pattern in academic dishonesty will lead to strong university-imposed penalties.

Attendance:
Attendance will be 5% weightage.

Accommodation:
If you have a disability, including a learning disability, for which you request disability support services/accommodation(s), please get in touch with the Disability Support Services office, so that the appropriate arrangements may be made. In accordance with the Federal Law, a student requesting disability support services/accommodation(s) must provide appropriate documentation of his/her disability to the Disability Support Services Counselor. For more information, call or visit the Student Accessibility and Resources Center located in the University Center, Room 3150. The Telephone number is 903.566.7079. Additional information may also be obtained at the following UT Tyler website: https://www.uttyler.edu/disabilityservices/

How to be Successful in this course:
The main focus of the Instructor is to help students learn the significant VLSI concepts. Some of the ways to be successful in this course are:

- Attend all the lectures during the class meeting time. Though the lectures will be recorded and published in Canvas, attending the live classes will help the students to interact with the Instructor and clarify their questions.
- Follow the deadlines. The course has 3 homework, 4 labs, 2 exams and reading assignment for assessment. Each of these have a weightage in the overall grade.
- Avoid plagiarism. In the event of any plagiarism, the particular assignment will not be graded resulting in "0". Its important that you submit original assignments to get credit for your work.
- WE ARE HERE TO HELP. If you have any questions or concerns related to this course, email the Instructor anytime or clarify the same during the class meeting hours or office hours.

Happy Learning!