The University of Texas at Tyler
Department of Electrical Engineering

CMPE 4332.001 and 040, EENG 4332.001 and 040: FPGA Design (Technical Elective)

Syllabus

Catalog Description:

Digital Systems design with Field Programmable Gate Arrays (FPGAs); Design and synthesis of reconfigurable logic with High-level Hardware Description Languages; Logic Design using FPGAs; Architectural and System Design issues; Reconfigurable computing with FPGAs. Three hours of lecture each week.

Prerequisites: EENG 3307 Microprocessors and EENG 4309 Electronic Circuits II or Consent of Instructor

Credits: 3 (3 hours lecture, 0 hours laboratory per week)

Text(s): Stephen Brown and Zvonko Vranesic, *Fundamentals of Digital Logic with Verilog Design.* 3rd Edition. Mc Graw Hill, 2014. ISBN 9780073380544

Additional Material: Peter J. Ashenden, The Student's Guide to VHDL. 2nd edition. Morgan Kaufmann, 2008.
Class Notes; Journal Articles

Course Coordinator: Prabha Sundaravadivel, AssociateProfessor

Topics Covered: (paragraph of topics separated by semicolons)

Digital system Design with FPGAs; Using CAD tools; Combinational and sequential Logic Design using FPGAs; Architectural issues; Fine-grained versus coarse-grained fabrics; Advance applications of FPGAs; System Design issues.

Evaluation Methods: (only items in dark print apply):

1. Examinations / Quizzes
2. Homework
3. Report
4. Computer Programming
5. Project
6. Presentation
7. Course Participation
8. Peer Review

Course Learning Outcomes[1]: By the end of this course students will be able to:

1. Explain how FPGAs are used in digital system design. [1,2]
2. Design digital logic circuits using Verilog and VHDL. [1,4,5]
3. Use CAD tools in the design, simulation, and implementation of FPGA designs. [3,4,5]
4. Analyze the implementation of reconfigurable logics in a VLSI process [1]
5. Design and implement Combinational and sequential logic circuits with FPGAs. [1,2,7]
6. Design and implement Finite State Machines using HDL [1,2,4]
7. Identify the issues at the architectural level associated with reconfigurable logic. [1,7]
8. Explore the real-time advance applications of FPGA boards. [3,6]
9. Explore the current research trend in FPGA. [6]

[1]*Numbers in brackets refer to method(s) used to evaluate the course learning outcome.*

Relationship to Student Outcomes (only items in dark print apply)[2]: This course supports the following Electrical Engineering Student Outcomes, which state that our students will possess:

1. An ability to identify, formulate, and solve complex engineering problems by applying principles of engineering, science, and mathematics [1,4,5].
2. An ability to apply engineering design to produce solutions that meet specified needs with consideration of public health, safety, and welfare, as well as global, cultural, social, environmental, and economic factors [6,2].
3. An ability to communicate effectively with a range of audiences [7].
4. An ability to recognize ethical and professional responsibilities in engineering situations and make informed judgments, which must consider the impact of engineering solutions in global, economic, environmental, and societal contexts [8].
5. an ability to function effectively on a team whose members together provide leadership, create a collaborative and inclusive environment, establish goals, plan tasks, and meet objectives
6. An ability to develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgment to draw conclusions [3].
7. An ability to acquire and apply new knowledge as needed, using appropriate learning strategies. [9].

[2]*Numbers in brackets refer to course learning outcome(s) that address the Program Outcome.*

Contribution to Meeting Professional Component: (in semester hours)

Mathematics and Basic Sciences:		hours
Engineering Sciences and Design:	3	hours
General Education Component:		hours

Grade Replacement:

If you are repeating this course for a grade replacement, you must file an intent to receive grade forgiveness with the registrar by the 12th day of class. Failure to file an intent to use grade forgiveness will result in both the original and repeated grade being used to calculate your overall grade point average. A student will receive grade forgiveness (grade replacement) for only three (undergraduate student) or two (graduate student) course repeats during his/her career at UT Tyler. (2006-08 Catalog, p. 35)

Prepared By:	Prabha Sundaravadivel, Associate Professor	Date:	15 January 2019
Edited By:			5 January 2026

The University of Texas at Tyler
Department of Electrical Engineering

Course: CMPE 4332.001 and 040 and EENG 4332.001, 040 – FPGA Design
COURSE OUTLINE

Course Coordinator:

Dr. Prabha Sundaravadivel
Associate Professor, Department of Electrical and Computer Engineering
Office: RBN 2015
Email: PSundaravadivel@uttyler.edu
Office Hours: T/ Thu 11 AM – 12:30 PM
Email and Canvas Discussion Boards.
Office hours Zoom ID: 93218434227
Passcode: Spring2026

Class Location/Time: Hybrid Model: Synchronous zoom classes and/or in-person.

T/Thu 5:00 PM- 6:20 PM,

Join Zoom Meeting:
https://uttyler.zoom.us/j/82495257619?pwd=bMpFO7hVOlyceRX0exYVqajR36KmPs.1

Meeting ID: 824 9525 7619
Passcode: Spring2026

Grading Policy:

Participation	5%	Attendance (5%)
Quizzes/Assignments	35%	occasional short assignments (FSM) or quiz, and engagement through discussions.
Reading Assignments	10%	1 Research Paper
Exams	50%	2 Exams
Total	**100%**	

Semester Schedule (tentative):

Week	Start Date	Topics Covered	Lecture (Tuesdays)	Lecture (Thursdays)
1	13-Jan	*Intro to FPGA*	Course Overview, Introduction to FPGA	Intro to FPGA architecture, development process
2	20-Jan	*Intro to FPGA design flow and HDLs*	Intro to logic circuits	Intro to FPGA design flow, HDLs
3	27-Jan	*Verilog*	Introduction	Boolean algebra, EDA tools
4	3-Feb	*Verilog*	Digital circuit design, Verilog coding	Verilog coding - basics
5	10-Feb	*Verilog*	Verilog coding - statements	**Exam-1**

6	17-Feb	*FSMs*	Mealy	Moore
7	24-Feb	*VHDL*	VHDL basics	VHDL - signals
8	3-Mar	*VHDL*	VHDL- statements	VHDL -examples
9	9 -Mar	**Spring Break**		
10	17-Mar	*Combinational Circuits*	Verilog examples	VHDL examples
11	24-Mar	*Sequential circuits*	Verilog examples	VHDL examples
12	31-Mar	*FPGA development*	Timing analysis (theory)	Hands-on
13	7-April	*FPGA implementation*	Case studies	Case studies
14	14-April	*Research paper review*	Research paper review	**Exam-2**
15	21-April	*FPGA implementations*	FSM Implementations	
16	28 April	*FPGA implementations*	VHDL-based designs – real-world implementations	

Mode of Delivery:

This course is a synchronous in-person course. *The first 3 weeks of the semester will be offered as online classes / recorded lectures due to work-related travel. The announcements will be made in advance in Canvas regarding the same.* Attendance is mandatory for all in-person sessions. It's the student's responsibility to review the given materials promptly and stay updated on weekly course content. Feel free to email the instructor with concerns or feedback about the lectures.

Flexible Online Office Hours:

Students can meet with the instructor during office hours on Tuesdays /Thursdays (11 -12:30) at her office in RBN 2015 or using the class Zoom link. However, if students are unavailable during the mentioned office hours, they are strongly encouraged to schedule a meeting with the Instructor anytime.

Short Assignment and Quiz:

There will be about 6-8 short assignments or quiz, after significant topics such as Finite State Machines, is discussed in the class. The purpose of this is to help in assessing the understanding of topics. About a week's time would be given for each assignment submission and quiz preparation. This will account for 35% of the grade. No late submissions will be accepted. Assignment problems/ questions may be discussed with other students, but the final submission should be an original and independent solution.

Research Reading Assignments:

One research paper will be assigned before the Mid-Term week. Students are expected to read the research paper and make a 10-minute presentation for each paper. This presentation will be reviewed on last 2 weeks of the course. The total of 10-minute video presentation along with the powerpoint slides will have 10% weightage.

Exam:

This course will have 2 exams with 20% weightage for each. There is no Final Exam for this course.

Academic Integrity:

Students should be aware that absolute academic integrity is expected of every student in all undertakings at the University of Texas at Tyler. A plagiarism check will be done all the reports submitted by students. Copied or unoriginal solutions will result in a "0" in that course component. An evidence of a pattern in academic dishonesty will lead to strong university-imposed penalties.

Attendance:

As an emphasis on consistent participation of students throughout the course, attendance will be taken after each class lecture.

Students Rights and Responsibilities

To know and understand the policies that affect your rights and responsibilities as a student at UT Tyler, please follow this link: http://www.uttyler.edu/wellness/rightsresponsibilities.php

Grade Replacement/Forgiveness and Census Date Policies:

Students repeating a course for grade forgiveness (grade replacement) must file a Grade Replacement Contract with the Enrollment Services Center (ADM 230) on or before the Census Date of the semester in which the course will be repeated. Grade Replacement Contracts are available in the Enrollment Services Center or at http://www.uttyler.edu/registrar. Each semester's Census Date can be found on the Contract itself, on the Academic Calendar, or in the information pamphlets published each semester by the Office of the Registrar.

Failure to file a Grade Replacement Contract will result in both the original and repeated grade being used to calculate your overall grade point average. Undergraduates are eligible to exercise grade replacement for only three course repeats during their career at UT Tyler; graduates are eligible for two grade replacements. Full policy details are printed on each Grade Replacement Contract.

The Census Date is the deadline for many forms and enrollment actions that students need to be aware of. These include:

- Submitting Grade Replacement Contracts, Transient Forms, requests to withhold directory information, approvals for taking courses as Audit, Pass/Fail or Credit/No Credit.
- Receiving 100% refunds for partial withdrawals. (There is no refund for these after the Census Date)
- Schedule adjustments (section changes, adding a new class, dropping without a "W" grade)
- Being reinstated or re-enrolled in classes after being dropped for non-payment
- Completing the process for tuition exemptions or waivers through Financial Aid

State-Mandated Course Drop Policy

Texas law prohibits a student who began college for the first time in Fall 2007 or thereafter from dropping more than six courses during their entire undergraduate career. This includes courses dropped at another 2-year or 4-year Texas public college or university. For purposes of this rule, a dropped course is any course that is dropped after the census date (See Academic Calendar for the specific date). Exceptions to the 6-drop rule may be found in the catalog. Petitions for exemptions must be submitted to the Enrollment Services Center and must be accompanied by documentation of the extenuating circumstance. Please contact the Enrollment Services Center if you have any questions.

Disability Services

In accordance with federal law, a student requesting accommodation must provide documentation of his/her disability to the Disability Services counselor. If you have a disability, including a learning disability, for which you request an accommodation, please contact the Disability Services office in UC 3150, or call (903) 566-7079.

Student Absence due to Religious Observance

Students who anticipate being absent from class due to a religious observance are requested to inform the instructor of such absences by the second class meeting of the semester.

Student Absence for University-Sponsored Events and Activities

If you intend to be absent for a university-sponsored event or activity, you (or the event sponsor) must notify the instructor at least two weeks prior to the date of the planned absence. At that time the instructor will set a date and time when make-up assignments will be completed.

Social Security and FERPA Statement:

It is the policy of The University of Texas at Tyler to protect the confidential nature of social security numbers. The University has changed its computer programming so that all students have an identification number. The electronic transmission of grades (e.g., via e-mail) risks violation of the Family Educational Rights and Privacy Act; grades will not be transmitted electronically.

Emergency Exits and Evacuation:

Everyone is required to exit the building when a fire alarm goes off. Follow your instructor's directions regarding the appropriate exit. If you require assistance during an evacuation, inform your instructor in the first week of class. Do not re-enter the building unless given permission by University Police, Fire department, or Fire Prevention Services.

Happy Learning!